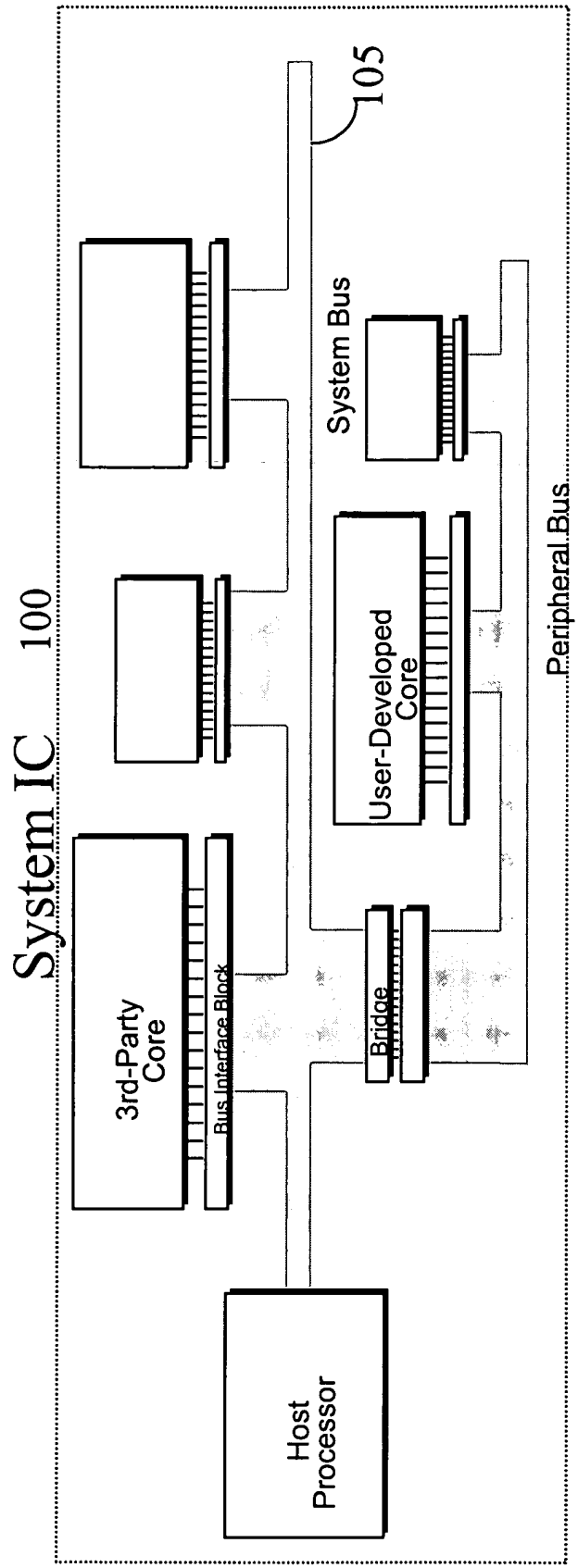

Figure 1a (prior art)

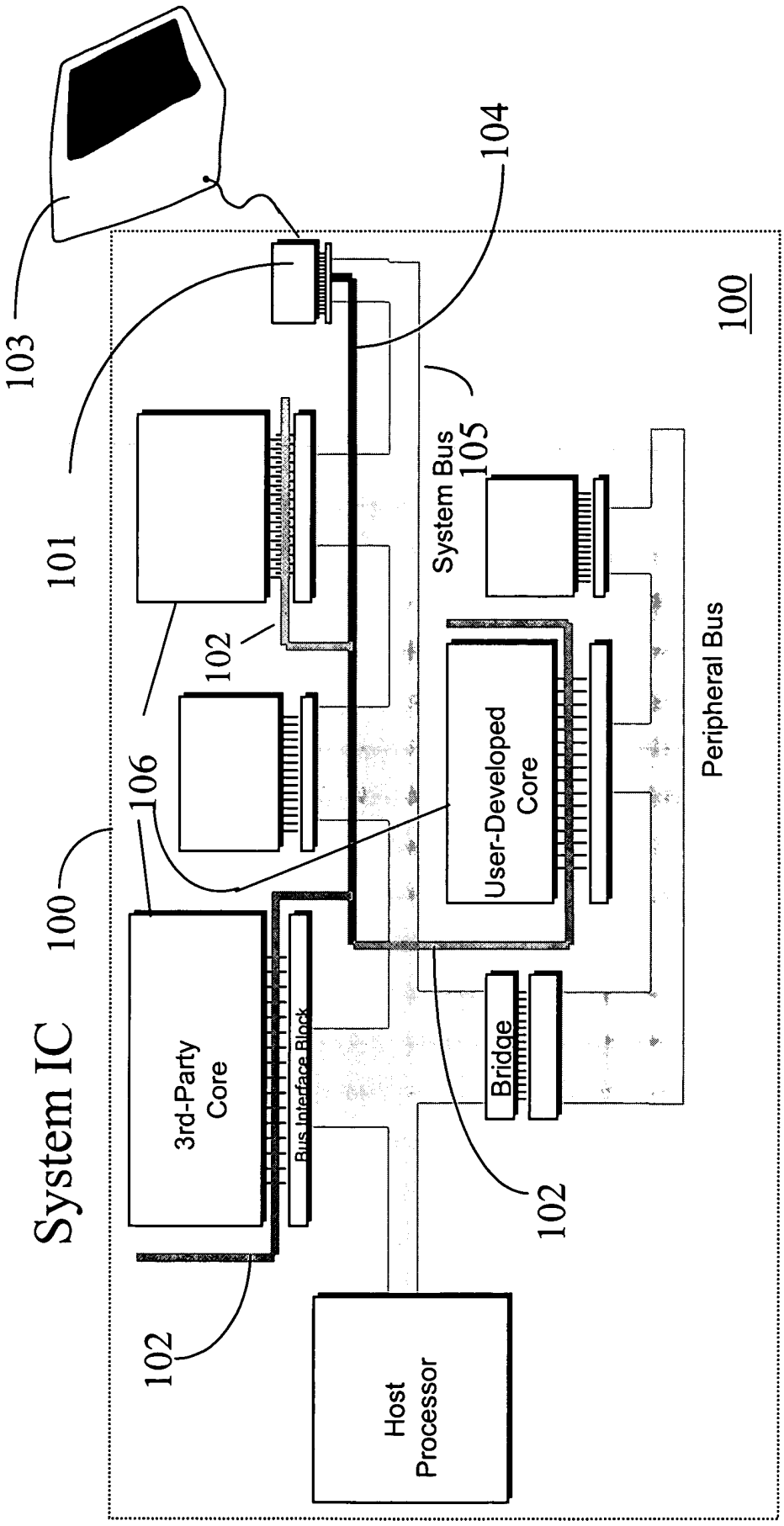
System IC
100
103
101
104
System Bus
105
102
106
3rd-Party Core
Bus Interface Block
User-Developed Core
Peripheral Bus
100
Bridge
102
102
Host Processor

Figure 1b

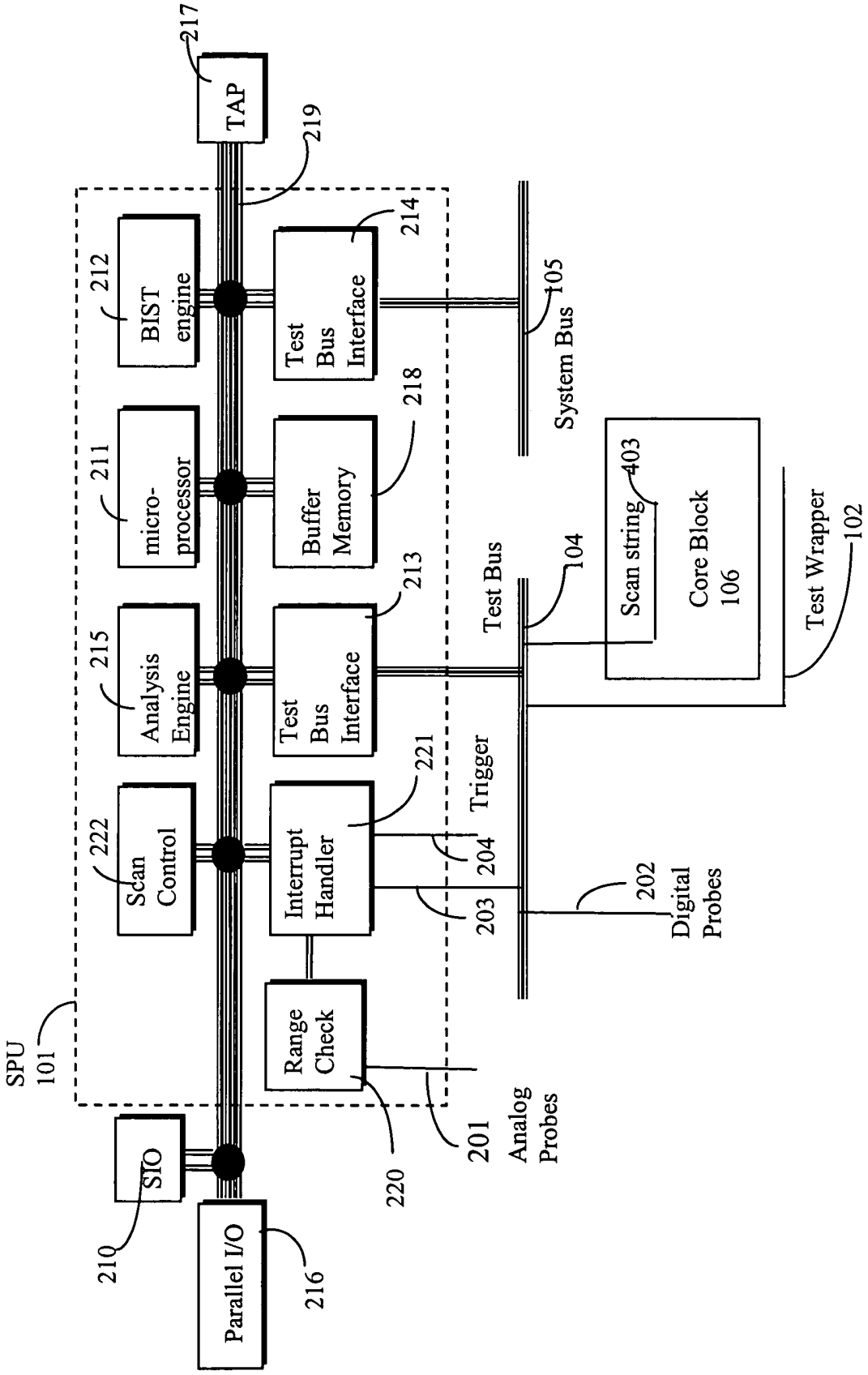
SPU
101
TAP
217
219
BIST engine
212
Test Bus Interface
214
System Bus
105
micro-processor
211
Buffer Memory
218
Scan string
403
Core Block
106
Test Wrapper
102
Analysis Engine
215
Test Bus Interface
213
Test Bus
104
Scan Control
222
Interrupt Handler
221
Trigger
204
203
202
Digital Probes
Range Check
220
201
Analog Probes
SIO
210
Parallel I/O
216

Figure 2

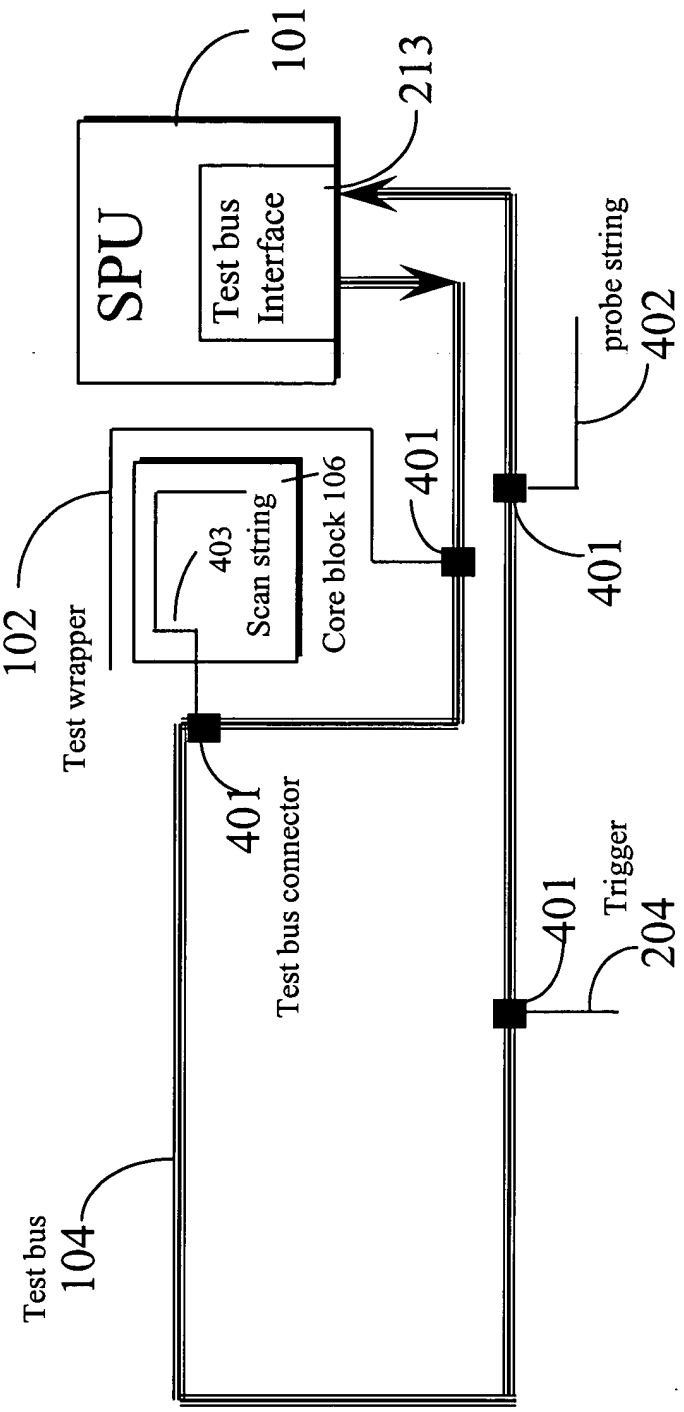
SPU
Test bus Interface
101
213
probe string
402
401
401
Core block 106
403
Scan string
102
Test wrapper
401
Test bus connector
401
Trigger
204
Test bus
104

Figure 3a

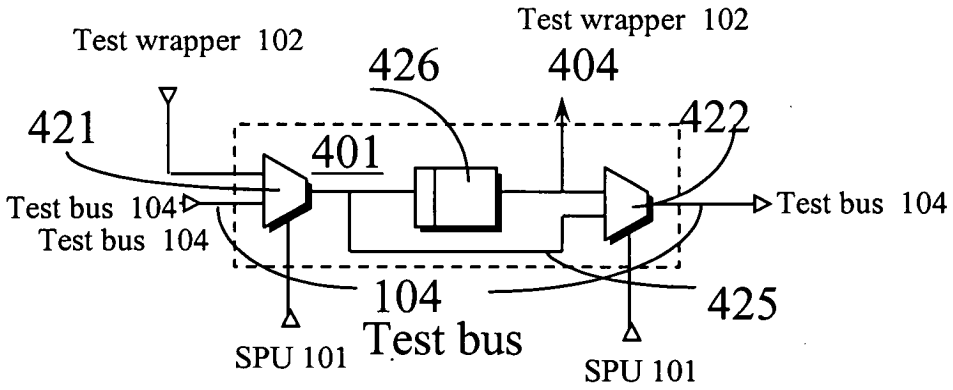

Figure 3b

Preferred Embodiment of Test Bus Connector

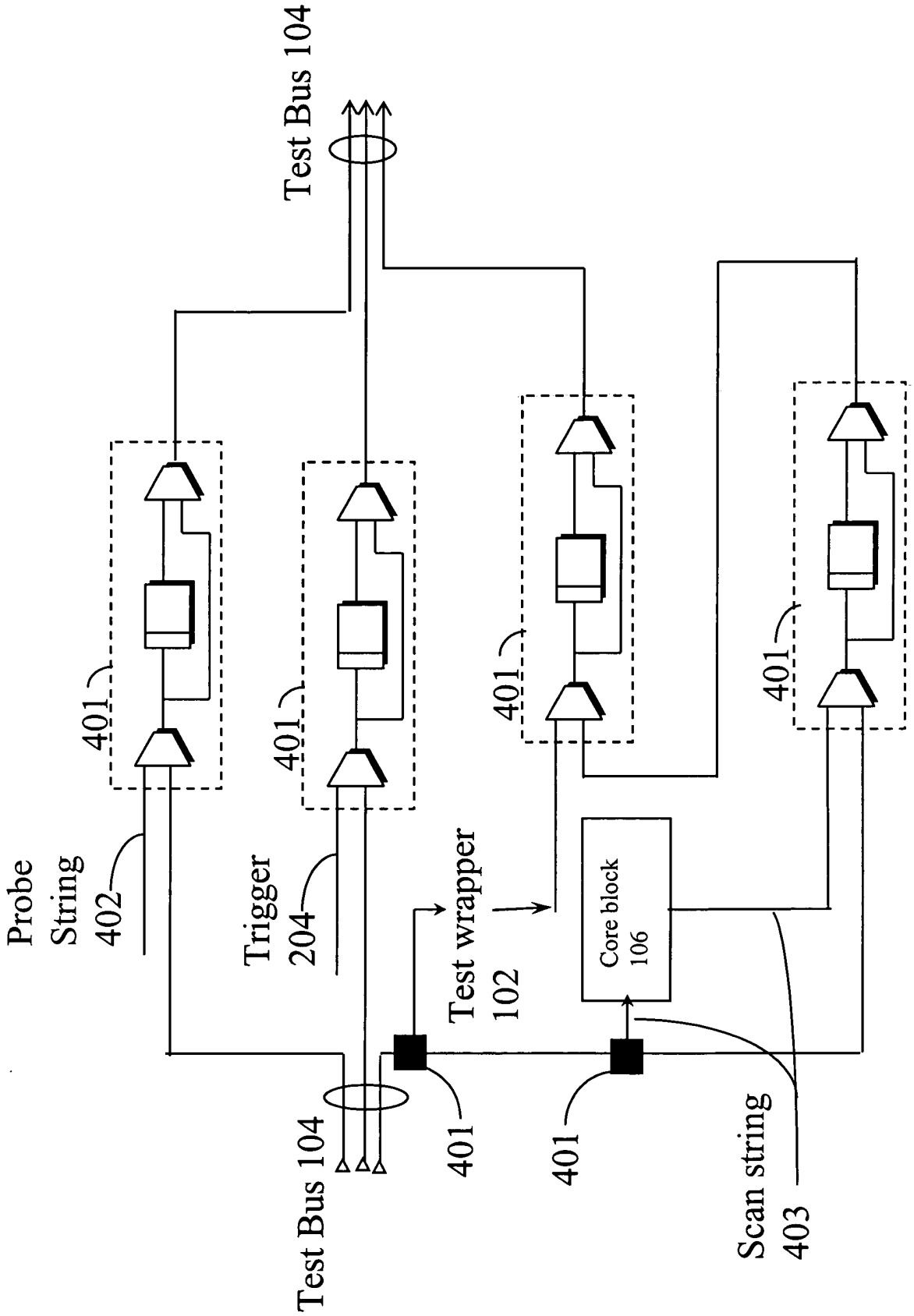

Figure 3c

Connecting Probe String, Test Wrapper or Scan String to Test Bus

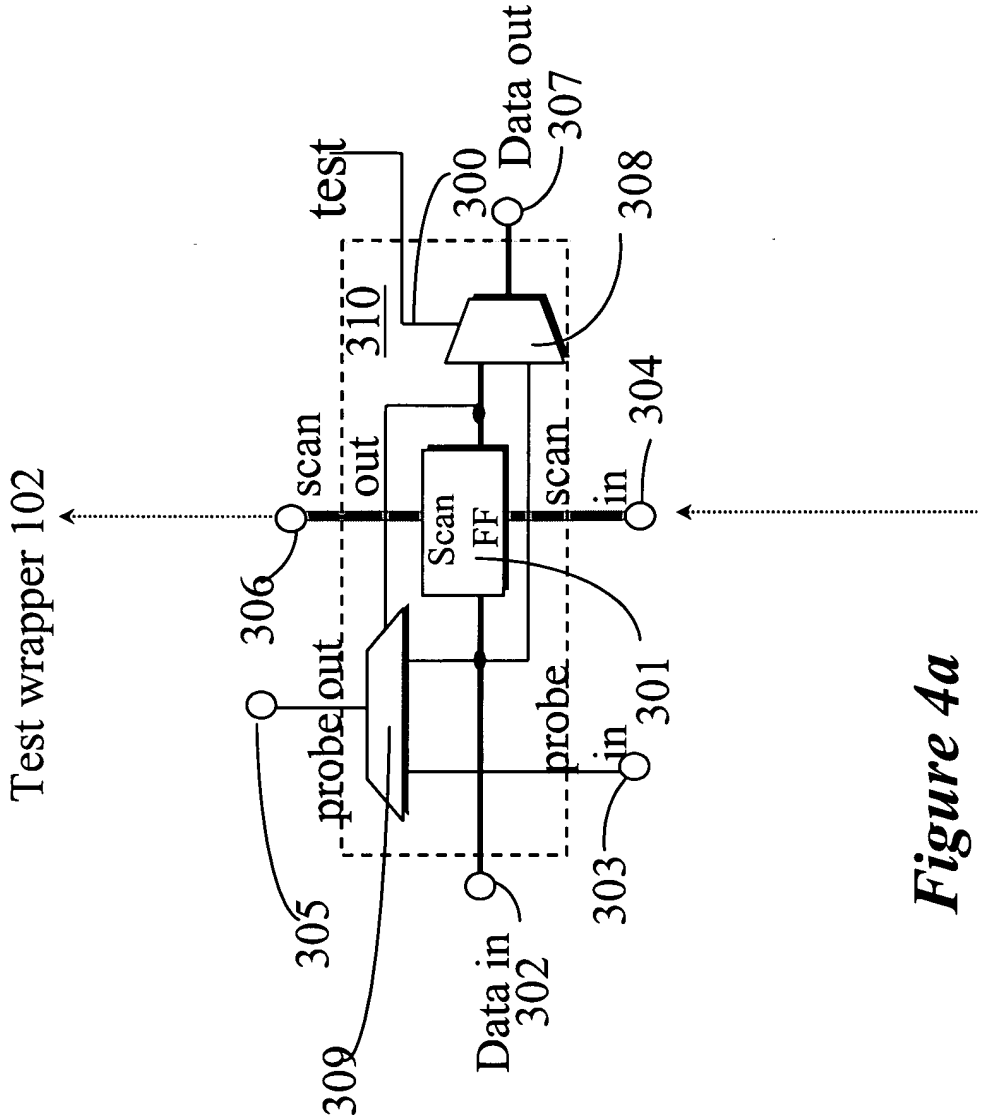

Figure 4a

Preferred Embodiment of Block Input/Output Port Connector

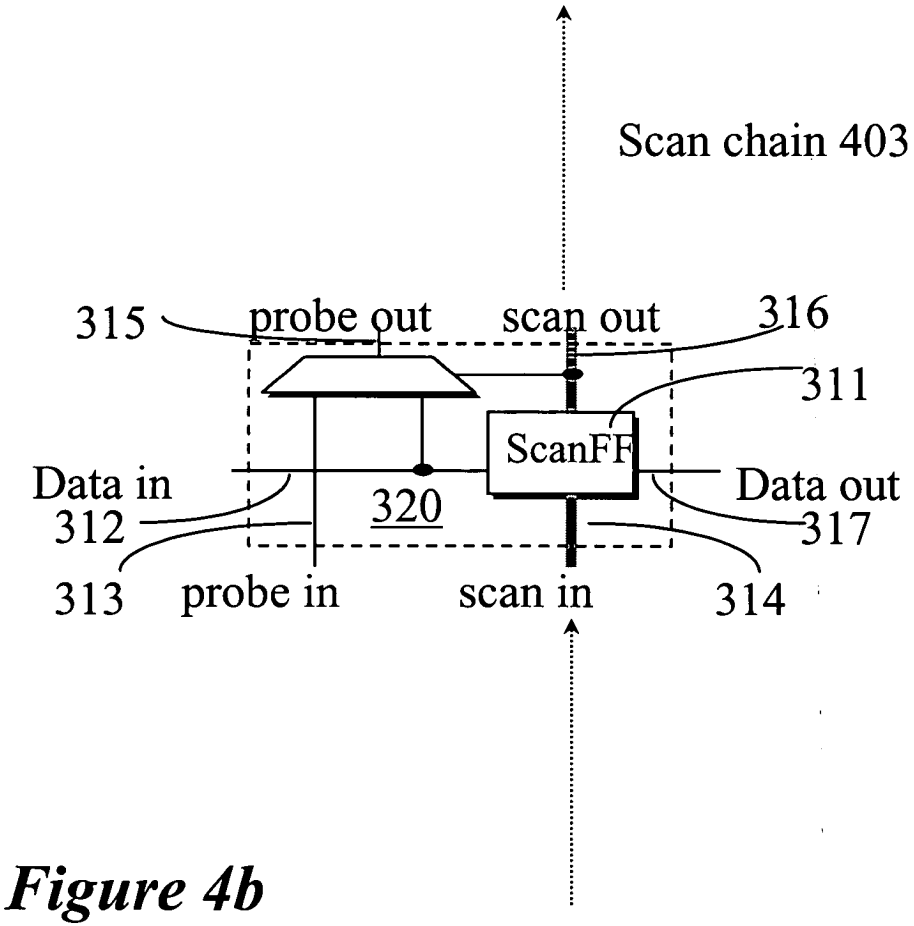

Figure 4b

Preferred Embodiment of Block Scan Connector

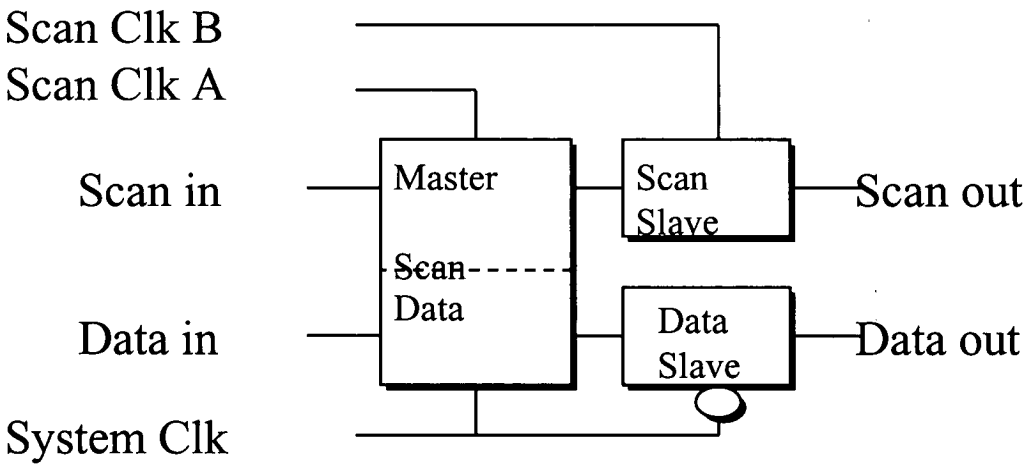

Figure 5

Internal Scan Element with Separate Scan-Slave and Data-Slave: (prior art)

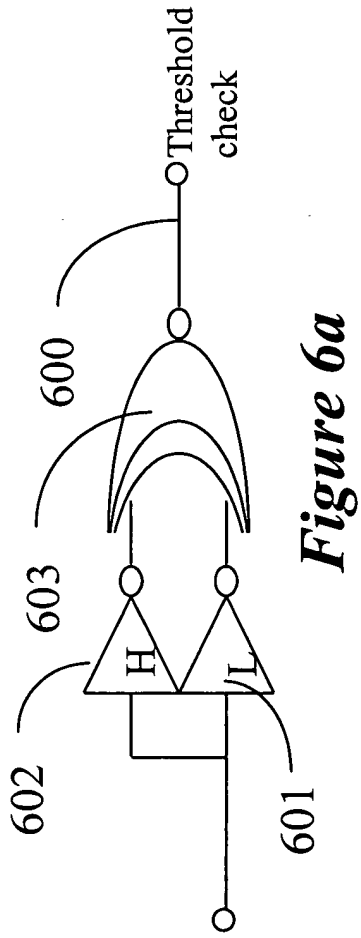

Figure 6a

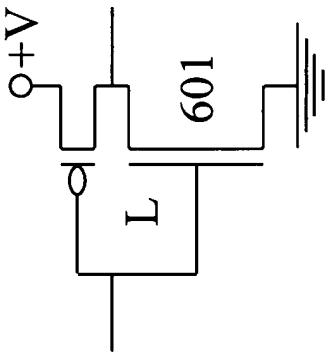

Figure 6b

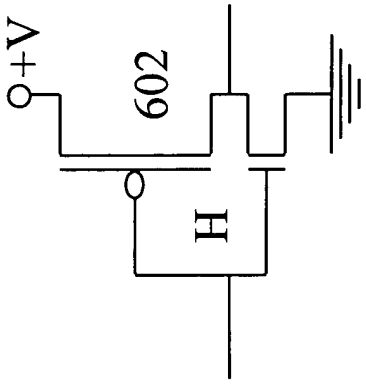

Figure 6c

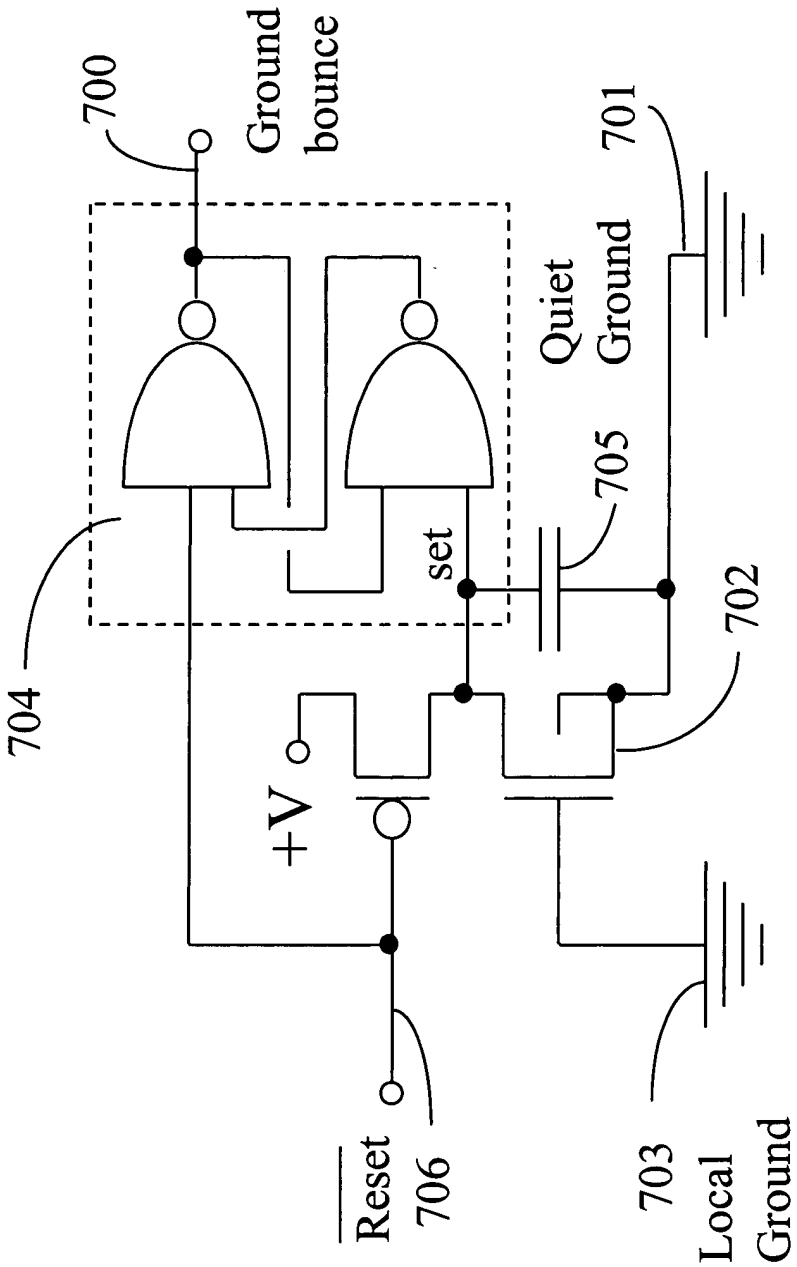
700
Ground bounce
701
Quiet Ground
705
set
704
+V
702
Reset
706
703
Local Ground

Figure 7

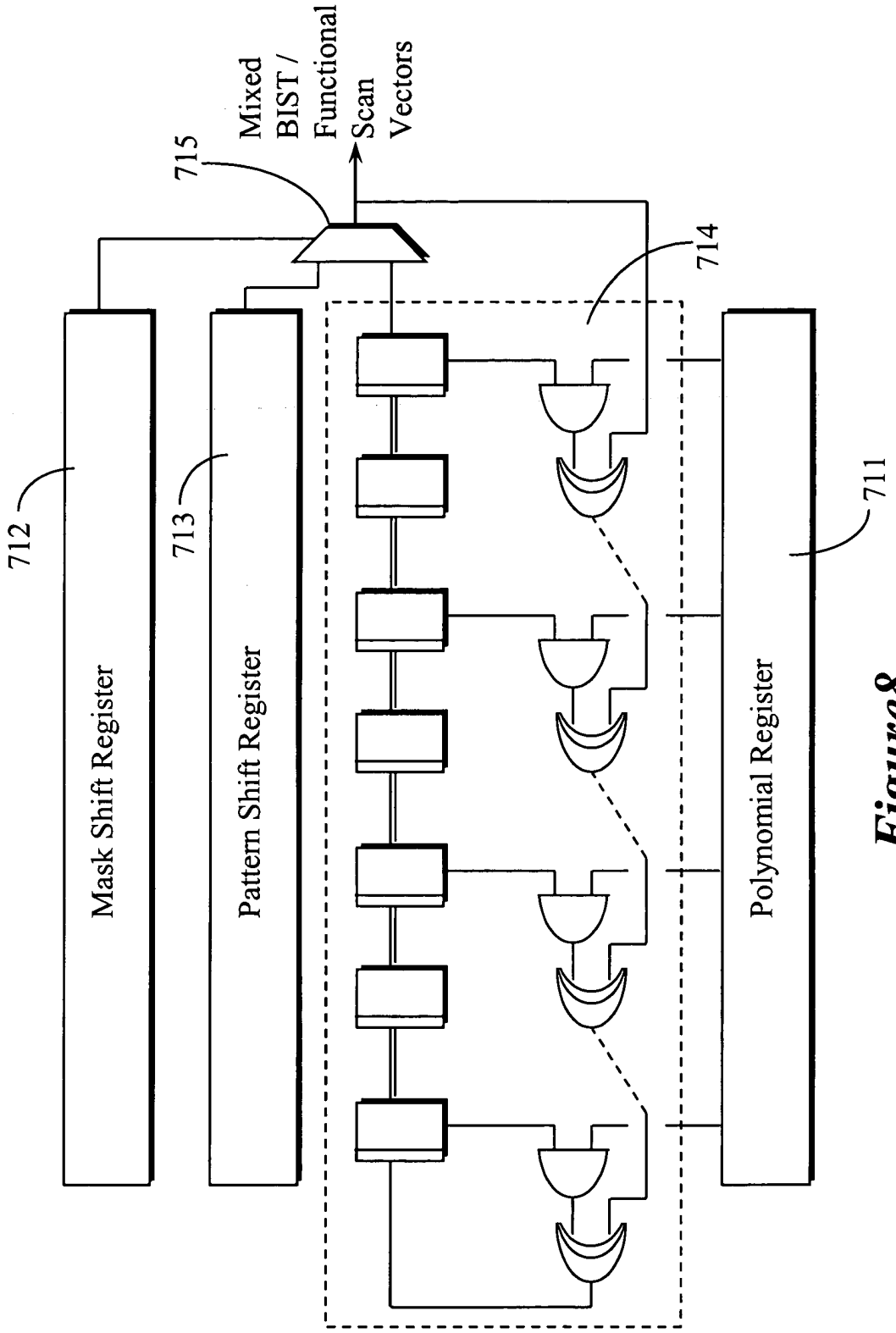
Mixed BIST / Functional Scan Vectors
715
714
712
713
711
Mask Shift Register
Pattern Shift Register
Polynomial Register

Figure8

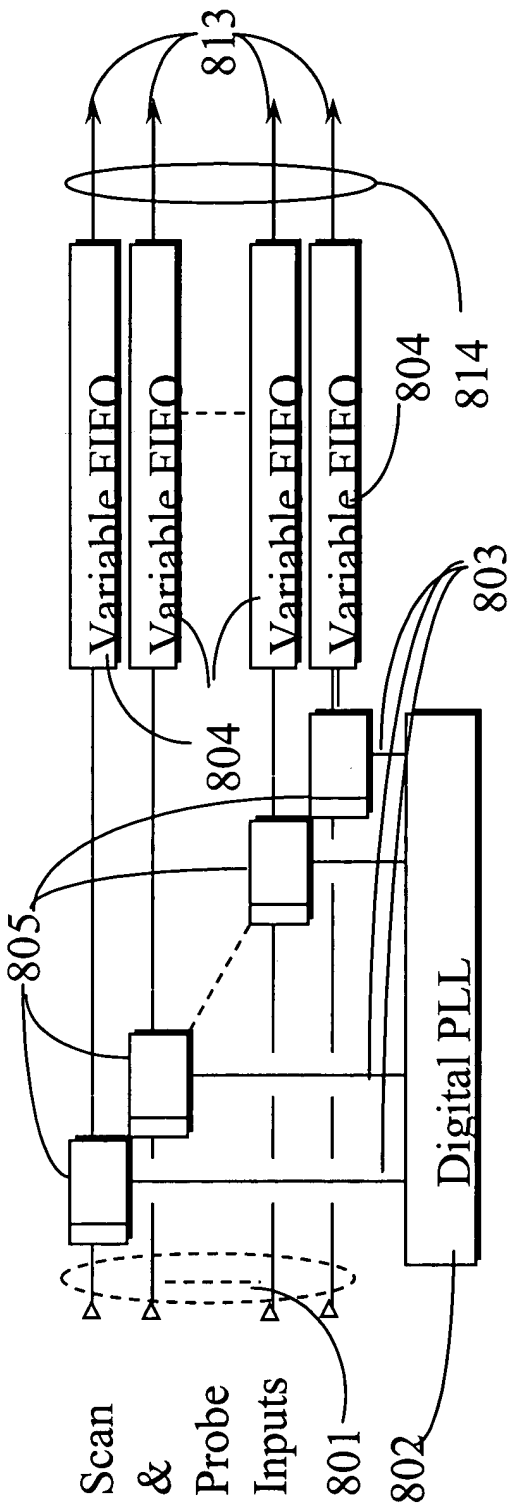

Figure 9a

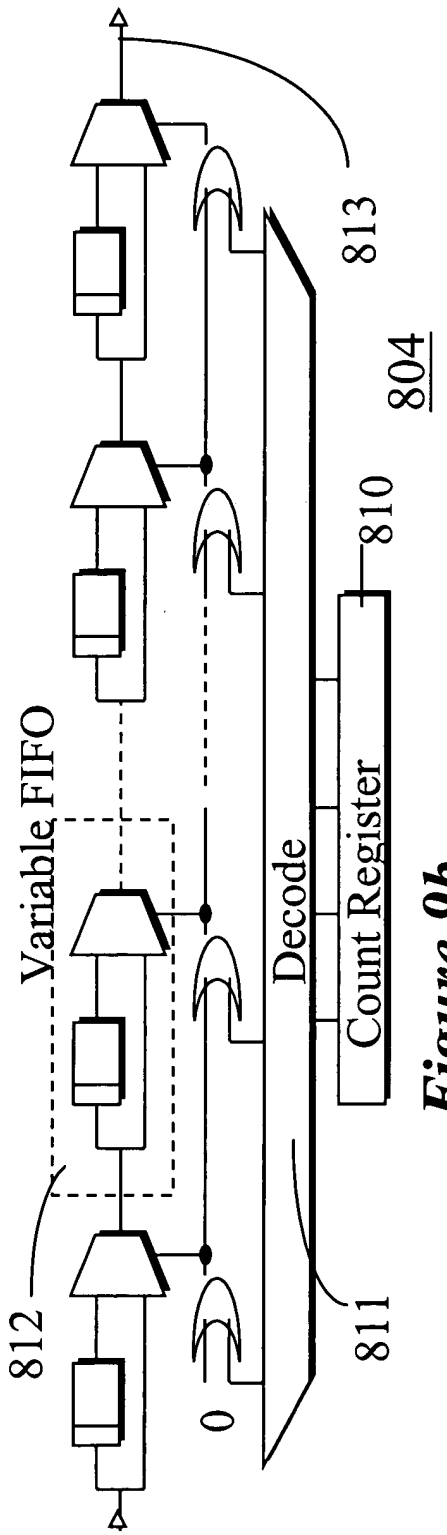

Figure 9b

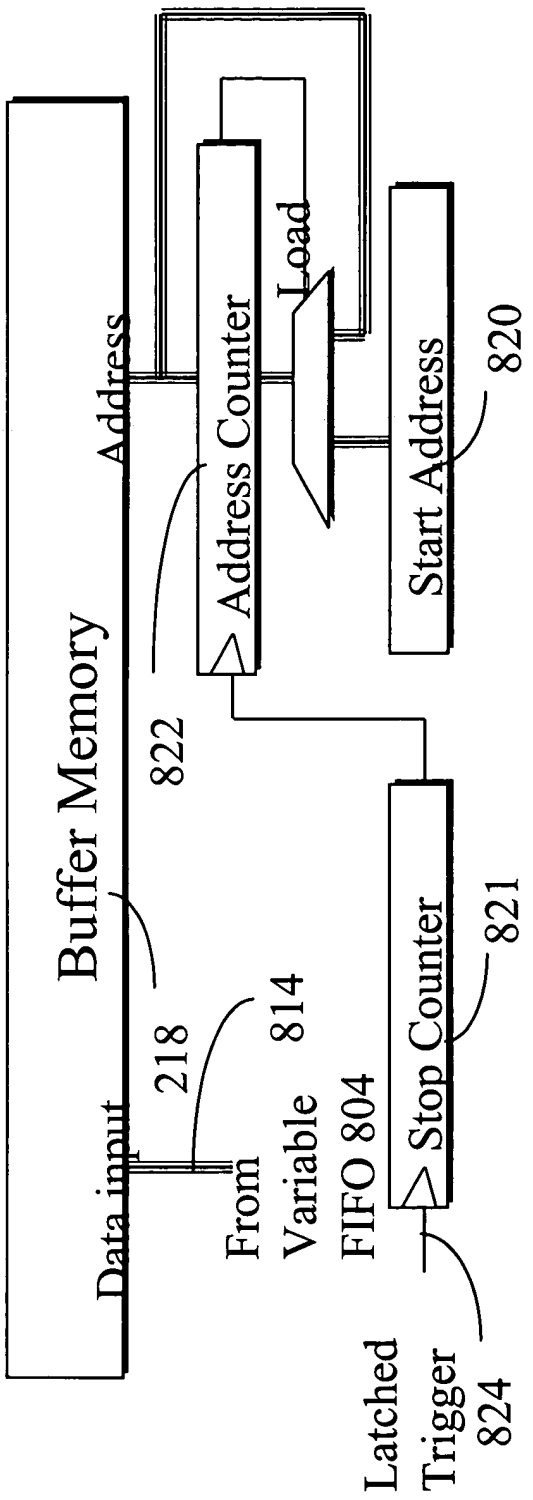

Figure 9c

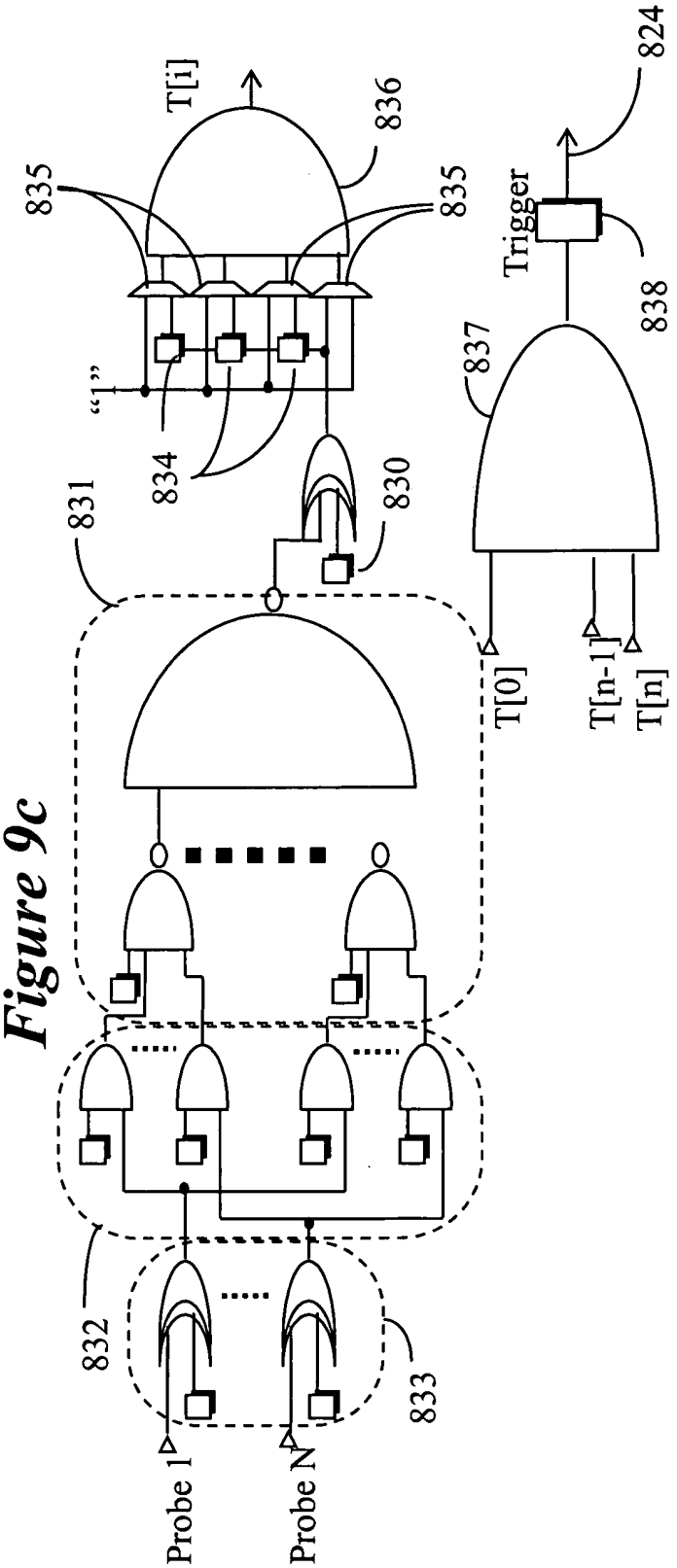

Figure 9d

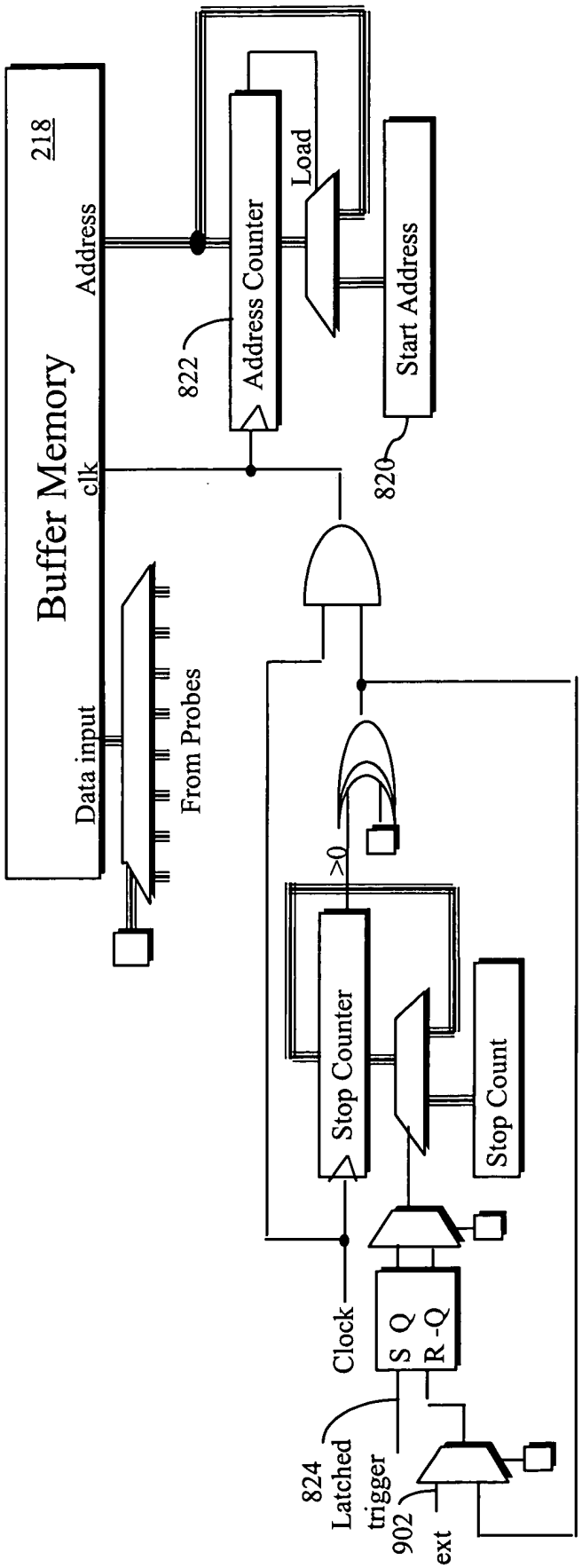

Figure 10

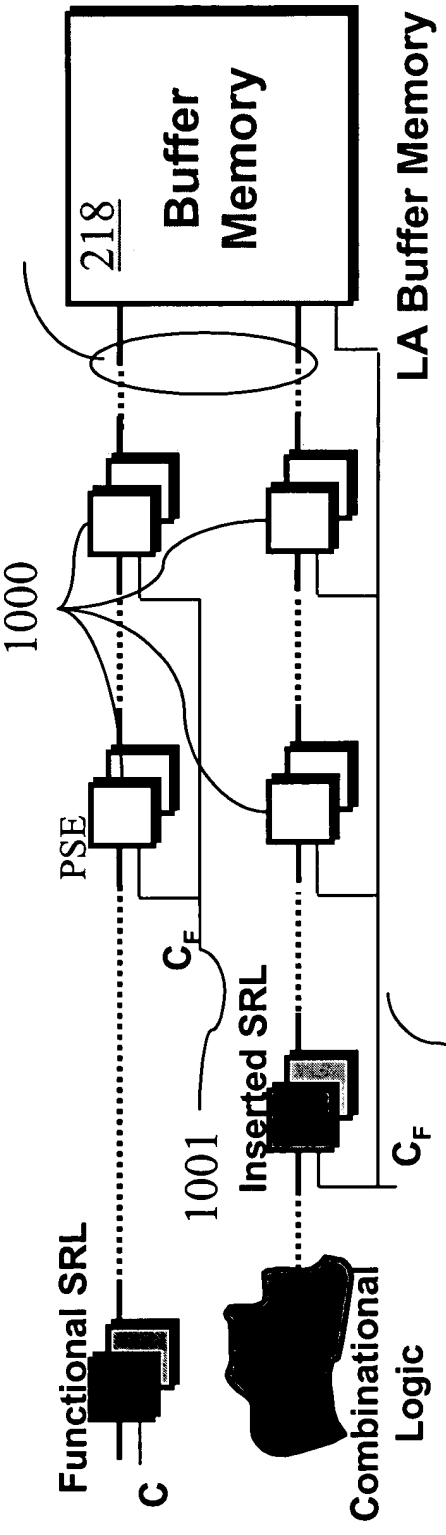

Figure 11

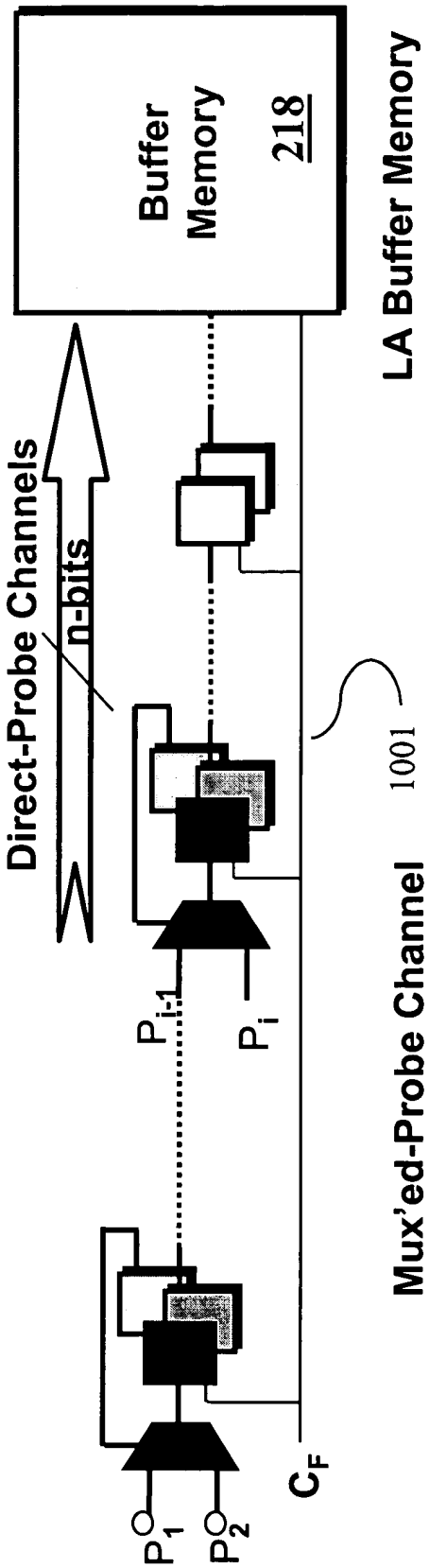

Figure 12

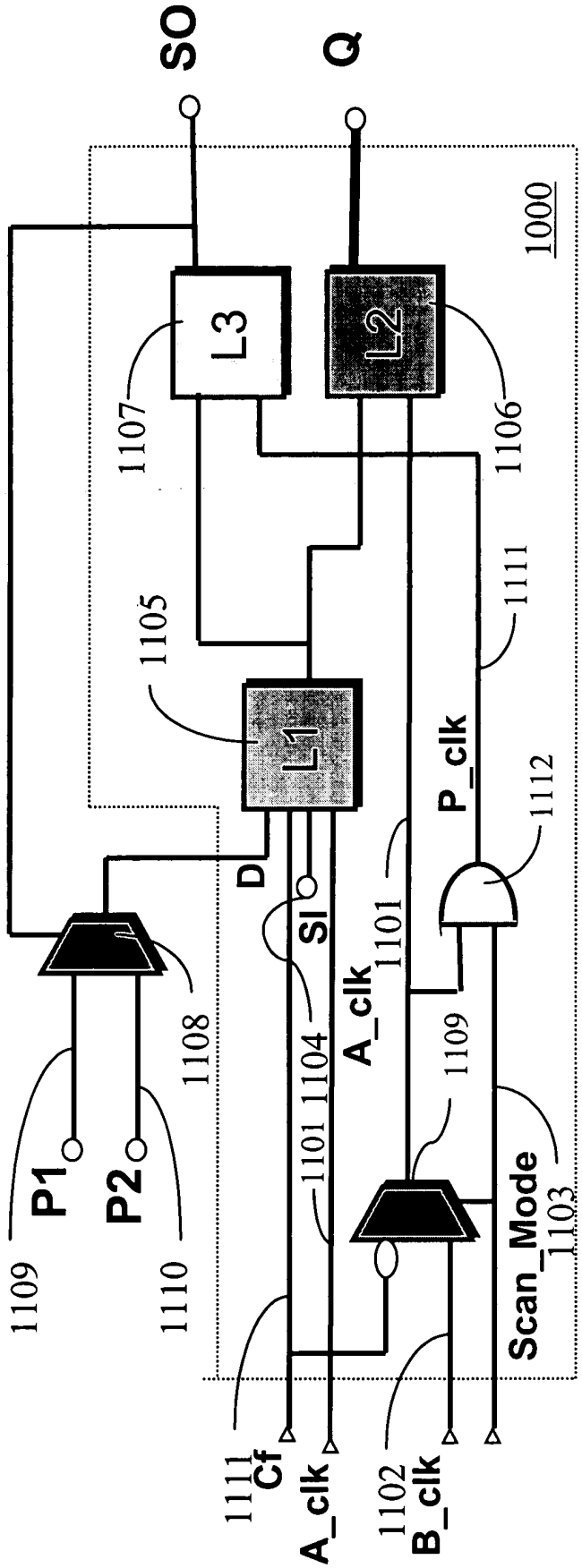

Figure 13